ABOUT THE INSTITUTION

The College is the brainchild of the renowned philanthropist, Sri G.PullaReddy Established in 1985 and managed by G. Pulla Reddy Charities Trust, the college is affiliated to Jawaharlal Nehru Technological University Anantapuramu and approved by AICTE, accredited by NBA of AICTE and NAAC of UGC.The College celebrated its Silver Jubilee celebrations during 2009-2010 and completed 39 years of its service in Engineering Education. The college offers Under Graduate Programs in Nine branches and Five Post Graduate courses. The college is situated on Kurnool-Chittoor National Highway No.7 Kurnool is well connected by Rail and Road. The places of ritmest nearby Srisailam, Alampur, Mahanand, Mentralayanand Belum Caves.

ABOUT THE DEPARTMENT

The Department of Electronics and Communication Engineering was established in the academic year 1984-85 with an intake of 40 and currently with 180 regular and 18 lateral entry students. The department is also offering one postgraduate programme with the specialization of VLSI and Embedded system with an intake of 12 students.

CHIEF PATRON Sri.P.Subba Reddy, Chairman, GPREC.

PATRON

Dr.B.Sreenivasa Reddy,

Principal, GPREC.

CO-PATRONS

Dr.S.Nagaraja Rao,

Prof.&HOD of ECE,GPREC.

Dr.K.Suresh Reddy,

Dr.K.Suresh Reddy,

Prof.&Associate HOD, ECE,GPREC.

CONVENOR

Dr M.Madhusudhan Reddy,

Asst.Professor,ECE,GPREC.

CO-ORDINATORS

Smt.W.Yasmeen,

Assistant Professor.

Smt.A.Parvathi,

Assistant Professor.

CO-COORDINATORS

Dr.G.Amjad Khan,

Associate Professor.

Dr.P.C.Praveen Kumar,

Assistant Professor.



ONE-WEEK NATIONAL LEVEL FACULTY
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December 03rd 07th, 2024



Department of Electronics & Communication Engineering

G PULLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

Accredited by NBA of AICTE & NAAC of UGC with A Grade G.Pulla Reddy Nagar, Nandyal Road, KURNOOL – 518 007, Andhra Pradesh,India. www.gprec.ac.in

ABOUT THE FDP

The objective is to impart quality training through Faculty Development Programmes (FDPs) for Research scholars and Faculty members.

The Objectives of the FDP:

The primary objective of this Faculty Development Program (FDP) provides participants an insight into the processes involved in taking a VLSI circuit concept to realization. Digital Design, Analog Design, DFT, Layout, Signal Processing for FPGAs will be covered. This ecosystem which is centralized provides an analytical sense of understanding of the design & required design variations/validations on top of existing methodologies. The participants will be basically trained to use Cadence EDA tools at industry requirements. For example, there is an exclusive Cadence PD flow for the back-end design. All the methodologies followed correlates with the mathematical equation. Very high standard EDA tools will be utilized for achieving industry standard specifications in this FDP.

EXPECTED OUTCOMES

Enhanced Knowledge:

Members of faculty can teach or deliver lectures by using EDA tools. This conceptualization makes students understand complex topics in easy manner.

Skill Development:

Members of faculty exposes to Signal Processing for FPGAs, Layout design with different nano meter(nm) technologies.

Curriculum Enrichment:

In the recent past, many new technologies have been introduced in the education system to reduce costs and increase efficiency. Same concepts are incorporated in curriculum development.

Professional Networking:

Faculty can connect professionals in the chip design industry and peer group connectivity becomes easier.

RESOURCE PERSONS

Mr. Basavaraj

Senior Technical Staff Maven Silicon Pvt Ltd , Bangalore.

Sri.Sudheer Kumar,

Application Engineer, Entuple Technologies Pvt Ltd, Bangalore.

> Dr. P Ranga Babu, Associate Professor, IIITDM Kurnool.

Dr M.Madhusudhan Reddy,

Assistant Professor, ECE, GPREC, Kurnool.

Advisory Committee

Dr.P.Abdul Khayum, Professor of ECE, GPREC. Dr.Shaik Saheb Basha, Professor of ECE, GPREC.

Dr. D R Srinivas

Assoc. Professor of ECE,GPREC. Dr.G Venkata Ramana Sagar

Assoc. Professor of ECE, GPREC.

Organizing Committee

Dr. S.M.Shamsheer Daula Associate Professor.

Dr.J.Salai Thillai Thilagam,

Associate Professor.

Smt.K.Lakshmi Devi,

Assistant Professor.

Sri S.Ramesh Babu,

Assistant Professor.

ELIGIBILITY

The faculty members, Research scholars & PG Students of the AICTE approved institutions, Industry professionals nominated by Heads of the Institutions

REGISTRATION FEE: ₹1000/-

REGISTRATION LINK:

https://bit.ly/FDP_VLSI



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